WHAT IS CLAIMED IS:

1. A method of electronically comparing two circuits for identicalness, comprising:

(a) compiling, within one or more memories, a first list of all components in a first circuit, said first list including data relative to all connections of each component listed, each component in said first list hereinafter being referred to as a vertex;

(b) compiling, within one or more memories, a second list of all components in a second circuit, said second list including data relative all connections of each component listed, each component in said second list hereinafter being referred to as a vertex;

(c) comparing, within one or more processors, each unique vertex in said first list with unique vertexes in said second list;

(d) removing matching vertexes from said first and second lists;

(e) generating, within one or more processors, a discrepancy listing of unmatched unique vertexes in said first and second lists;

(f) removing the unique vertexes from said first and second lists that were placed in the discrepancy listing;

(g) compiling, within one or more memories, new first and second lists of all remaining vertexes of previous first and second lists expanded in scope by one vertex attached to each connection of the previous list stored;

(h) comparing, within one or more processors, each unique vertex in said new first list with unique vertexes in said new second list;

(i) removing matching vertexes from said first and second lists;

(j) adding to said discrepancy listing any remaining unmatched unique vertexes in said new first and second lists;

(k) removing the unique vertexes from said new first and second lists that were added to the discrepancy listing in step (j); and

(l) repeating steps (g) through (k) until all vertexes have been uniquely defined.

2. A method of electronically comparing two circuits, using one or more processors, each comprising a plurality of components, for identicalness where each component commences a generated vertex having a scope of N, where a vertex having N=0 comprises a component with no other components attached to the component's connections and a vertex having N=1 comprises a component with one additional component connected to each connection of prime component, and so forth, comprising the steps of:

(a) compiling an initial first list, within one or more memories, of all vertexes in a first circuit wherein N=0;

(b) compiling an initial second list, within the one or more memories,of all vertexes in a second circuit wherein N=0;

(c) removing all unique vertexes that have a corresponding vertex in both said first and second lists;

(d) transferring all remaining unique vertexes in said first and second lists to a discrepancy list within the one or more memories;

(e) compiling new first and second lists, within the one or more memories, of all remaining vertexes wherein N is incremented by "1";

(f) removing all unique vertexes that have a corresponding vertex in both said new first and second lists;

(g) transferring all remaining unique vertexes in said

first and second lists to said discrepancy list; and

(h) repeating steps (e), (f) and (g) until all vertexes are removed from said lists.

3. A method of electronically ascertaining the identicalness of first and second circuits, comprising:

(a) creating, by one or more processors, first and second lists of signatures for all vertexes in first and second circuits respectively, the signatures having a given minimal scope and stored in one or more memories;

(b) deleting any vertexes from further consideration whose signatures are unique and appear identically in both said first and second lists;

(c) transferring a prime component, of any unique signatures, in either of said first and second lists to a discrepancy list stored in the one or more memories;

(d) deleting any vertexes from further consideration whose prime component has been transferred to said discrepancy list;

(e) creating, by the one or more processors, a revised first and second list of signatures for all remaining vertexes in first and second circuits respectively, after incrementing the scope of the signature;

(f) removing any vertexes from further consideration whose signatures are unique and appear identically in both said revised first and second lists;

(g) transferring a prime component, of any unique signatures, in either of said revised first and second lists to said discrepancy list stored in the one or more memories;

(h) removing any vertexes from further consideration by whose prime component has been transferred to said discrepancy list; and

(i) repeating steps (e) through (h) until all vertexes

have been removed from further consideration.

4. A method of electronically ascertaining the identicalness of first and second circuits, comprising:

(a) creating, within one or more memories, a first and second list of signatures for vertexes in first and second circuits respectively, the signatures having a given initial scope;

(b) deleting, within the one or more memories, any vertexes from further consideration whose signatures are unique and appear in both said first and second lists;

(c) transferring a prime component, of any remaining unique signatures, to a discrepancy list;

(d) creating, within the one or more memories, revised first and second lists of increased scope signatures for all remaining vertexes in first and second circuits;

(e) removing any vertexes from further consideration whose signatures are unique and appear identically in both said revised first and second lists;

(f) transferring a prime component, of any remaining unique signatures, to said discrepancy list; and

(g) repeating steps (d) through (f) until all vertexes have been removed from further consideration.

5. A computer program product for ascertaining the identicalness of two circuits, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

(a) computer code for creating first and second lists of signatures for vertexes in first and second circuits respectively, the signatures having a given initial scope;

(b) computer code for deleting any vertexes from further

consideration whose signatures are unique and appear in both said first and second lists;

(c) computer code for transferring a prime component, of any remaining unique signatures, to a discrepancy list;

(d) computer code for creating revised first and second lists of increased scope signatures for all remaining vertexes in the first and second circuits;

(e) computer code for removing any vertexes from further consideration whose signatures are unique and appear identically in both said revised first and second lists;

(f) computer code for transferring a prime component, of any remaining unique signatures, to said discrepancy list; and

(g) computer code for repeating steps (d) through (f) until all vertexes have been removed from further consideration.

6. Apparatus for electronically ascertaining the identicalness of two circuits, comprising:

(a) computation means;

(b) first and second lists of signatures for vertexes in first and second circuits respectively, the signatures having a given initial scope and stored within one or more memories;

(c) means, comprising a part of said computation means, for deleting any vertexes from further consideration whose signatures are unique and appear in both said first and second lists;

(d) means, comprising a part of said computation means, for transferring a prime component, of any remaining unique signatures, to a discrepancy list;

(e) means, comprising a part of said computation means, for creating revised first and second lists of increased scope signatures for all remaining vertexes in said two circuits;

(f) means, comprising a part of said computation means,

for removing any vertexes from further consideration whose signatures are unique and appear identically in both said revised first and second lists;

(g) means, comprising a part of said computation means, for transferring a prime component, of any remaining unique signatures, to said discrepancy list; and

(h) means, comprising a part of said computation means, for repeating steps (e) through (g) until all vertexes have been removed from further consideration.

7. A system for electronically computing Isomorphic graphs, comprising:

(a) graphical representations of two electrical circuits to be compared for identicalness by at least one processor;

(b) list creation means operable to create first and second lists of signatures for vertexes in first and second circuits respectively, the signatures having a given initial scope;

(c) detection means operable to delete any vertexes from further consideration whose signatures are unique and appear in both said first and second lists;

(d) removal means operable to transfer a prime component, of any remaining unique signatures, to a discrepancy list;

(e) creation means operable to create revised first and second lists of increased scope signatures for all remaining vertexes in said two circuits;

(f) further detection means operable to remove any vertexes from further consideration whose signatures are unique and appear identically in both said revised first and second lists;

(g) transfer means operable to transfer a prime component, of any remaining unique signatures, to said discrepancy list;

and

(h) repeating means operable to repeat steps (e) through (g) until all vertexes have been removed from further consideration.